3. The circuit of claim 1 wherein N=8.

4. (Amended) A circuit for providing multiple clock signals phase shifted from each other, the circuit comprising:

a phase lock loop circuit comparing an input signal and an error signal and providing an output signal; and

a multi-stage counter connected in the feedback path of the phase lock loop circuit to receive as an input the output signal of the phase lock loop circuit and providing an output signal as the error signal to the phase lock loop circuit; said counter also connected for providing at least two output signals from each of the stages of the counter as clock signals each having a phase displaced from the phase of the input signal <u>by a fixed angle</u>.

5. The circuit of claim 4 wherein the multi-stage counter is a Johnson counter having N stages and where the frequency of the output signal of the multi-stage counter is the frequency of the output signal of the phase lock loop circuit divided by 2N.

6. A circuit for receiving an input clock signal and generating a plurality of clock signals having frequencies identical to the input clock signal and predetermined phase displacements from the input signal, comprising:

a phase detector for comparing an input clock signal to a feedback signal and providing an output signal;

a low pass filter and gain stage receiving the output signal from the phase comparator and producing a control signal;

a voltage controlled oscillator for receiving the control signal and producing an oscillator output signal having a frequency corresponding to the control signal; and

a multistage counting circuit connected to receive the oscillator output signal and provide the feedback signal to the phase detector and a plurality of clock signals at the frequency of the input clock signal and phase shifted from the clock signal by fixed angular increments.

7. The circuit of claim 6 wherein the output signal of the phase detector corresponds to the phase difference between the input clock signal and the feedback signal.

8. The circuit of claim 6 wherein the frequency of the voltage controlled oscillator output signal is a multiple of the frequency of the input clock signal.

9. The circuit of claim 8 wherein multistage counting circuit is a Johnson counter having N stages.

11. (Amended) A circuit for generating multiphase clock signals, the circuit comprising:

a clock generator for generating a first clock signal at a clock frequency F_0;

a phase lock loop circuit receiving the first clock signal and providing an output signal; and

a Johnson counter having N stages connected to receive as an input the output signal of the phase lock loop circuit and providing an output signal as an error signal to the phase lock loop circuit; said Johnson counter also connected for providing output signals from each of the N stages of the Johnson counter as further clock signals, the output signals phase shifted from the first clock signal by a fixed angular increment.

12. The circuit of claim 11 wherein the output signal of the phase lock loop circuit has a frequency of 2N* F_0.

Please cancel claim 13 without prejudice.

13. (Canceled) A multiphase signal generator circuit, comprising:

a generator for generating a clock signal having a clock frequency;

a phase detector for comparing the clock signal to a feedback signal and providing an output signal;

a low pass filter and gain stage receiving the output signal from the phase

comparator and producing a control signal;

a voltage controlled oscillator for receiving the control signal and producing an oscillator output signal having a frequency corresponding to the control signal; and

a multistage counting circuit connected to receive the oscillator output signal and provide the feedback signal to the phase detector and a plurality of clock signals at the clock frequency and phase shifted from the clock signal.

14. (Amended) A multiphase signal generator circuit, comprising:
a generator for generating a clock signal having a clock frequency;

a phase detector for comparing the clock signal to a feedback signal and providing an output signal;

a low pass filter and gain stage receiving the output signal from the phase comparator and producing a control signal;

a voltage controlled oscillator for receiving the control signal and producing an oscillator output signal having a frequency corresponding to the control signal; and

a multistage counting circuit connected to receive the oscillator output signal and provide the feedback signal to the phase detector and a plurality of clock signals at the clock frequency and phase shifted from the clock signal [The circuit of claim 13 wherein the plurality of clock signals from the multistage counting circuit are shifted from each other] by fixed angular increments.

15. (Amended) The generator circuit of claim [13] 14 wherein the multistage counting circuit is a Johnson counter having N stages.

16. (Amended) The circuit of claim [13] 14 wherein the output signal of the phase detector corresponds to the phase difference between the input clock signal and the feedback signal.

17. (Amended) The circuit of claim [13] 14 wherein the frequency of the voltage controlled oscillator output signal is a multiple of the frequency of the input clock signal.

19. The circuit of claim 9 wherein the frequency of the voltage controlled oscillator output signal is a multiple of the frequency of the input clock signal.

20. A method for generating at least two clock signals displaced from each other by a predetermined phase shift of 360°/2N, where N is a positive integer, the method comprising:

applying a clock signal to a signal input of a phase lock loop circuit at the desired clock frequency;

applying a feedback signal to the other input of the phase lock loop;

generating an output of the phase lock loop having a frequency of 2N

coupling the output of the phase locked loop to an N stage Johnson counter to provide a signal to the other input of the phase lock loop having a frequency corresponding to the frequency of the output signal of the phase locked loop divided by 2N; and

coupling the outputs of the stages of the Johnson counter for use as phase shifted clock outputs.

21. The method of claim 20 wherein N=4.

REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on June 4, 2002, and the documents cited therewith.

Applicant has proposed that claims 4, 11 and 14-17 be amended, added no claims, and canceled claim 13; as a result, claims 1-9, 11, 12 and 14-17 and 19-21 are now pending in this application.

Allowed Claims

Claims 1-3, 6-9, 20 and 21 are allowed